# High Voltage, Isolated MOSFET Driver

#### **Features**

- ▶ ±400V input to output isolation
- ► Low input logic current, 500µA max
- ► No external voltage supply required
- ► Floating isolated output drivers
- ▶ 5.0V logic compatible

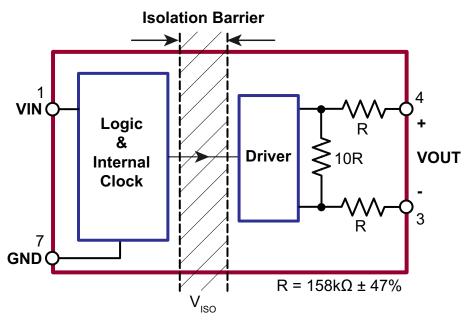
#### **Applications**

- ▶ Telecommunications
- ▶ Modems
- Solid state relays
- High side switches
- ► High end audio switches
- Avionics
- ► ATE

#### **General Description**

The Supertex HT0740 is a single channel, high voltage, low input current, isolated driver utilizing Supertex's proprietary HVCMOS® technology. It is designed to drive discrete MOSFETs, configured as high side switches, up to 400V. The HT0740 generates an independent DC isolated voltage across the pair of outputs when the logic input is at a logic high. The HT0740 does not require any external power supplies. The internal supply voltage is supplied from the logic input when it is in the high state.

### **Block Diagram**



## **Ordering Information**

Part Number	Package Option	Packing		
HT0740LG-G	8-Lead SOIC (Narrow Body)	2500/Reel		

<sup>-</sup>G denotes a lead (Pb)-free / RoHS compliant package

## **Absolute Maximum Ratings**

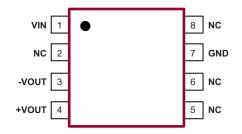
Parameter	Value
Input to output isolation voltage, $V_{\rm ISO}$	±400V
Logic input voltage, V <sub>IN</sub>	-0.5 to +7.0V
Operating temperature	-40°C to +85°C
Storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## **Typical Thermal Resistance**

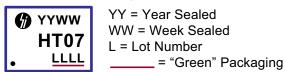
Package	$ heta_{ja}$
8-Lead SOIC (Narrow Body)	101°C/W

#### **Pin Configuration**



8-Lead SOIC (Narrow Body) (top view)

#### **Product Marking**



Package may or may not include the following marks: Si or

8-Lead SOIC (Narrow Body)

#### **Recommended Operating Conditions**

Sym	Parameter	Min	Тур	Max	Units	Conditions
V <sub>IH</sub>	Logic input high voltage	3.15	-	5.5	V	
V <sub>IL</sub>	Logic input low voltage	0	-	0.5	V	
T <sub>A</sub>	Operating temperature	-40	-	+85	°C	

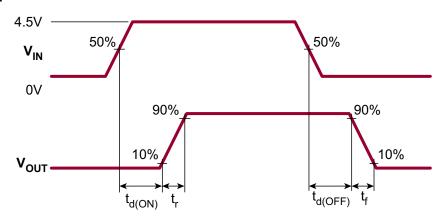
#### **DC Electrical Characteristics**

I <sub>H</sub>	Logic high input current	-	-	500	μA	V <sub>IN</sub> = 5.0V
IL	Logic low input current (quiescent)	-	-	10	μA	V <sub>IN</sub> = 0.5V
V	Output valtage geroes output terminals	4.5	-	-	V	V <sub>IN</sub> = 3.15V, no load
V <sub>OUT</sub> C	Output voltage across output terminals	8.5	-	-	V	V <sub>IN</sub> = 4.50V, no load
V <sub>IN</sub>	Input voltage for zero output	-	-	0.8	V	No load
V <sub>ISO</sub>	Input to output isolation voltage	±400	-	-	V	

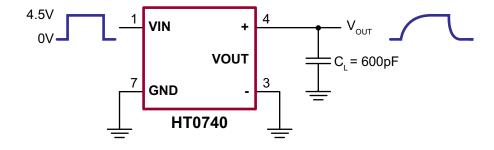
#### **AC Electrical Characteristics**

t <sub>d(ON)</sub>	Turn-on delay time	-	-	50	μs	
t <sub>r</sub>	Rise time	-		650	μs	See timing diagram and test
t <sub>d(OFF)</sub>	Turn-off delay time	-	-	150	μs	circuit $C_1 = 600 \text{pF}, T_A = 25^{\circ}\text{C}$
t,	Fall time	-	-	3.0	ms	, ,

# **Timing Diagram**

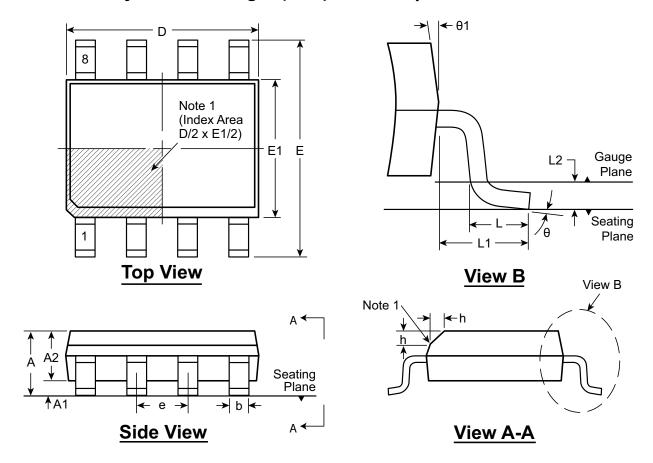


# **Test Circuit**



# 8-Lead SOIC (Narrow Body) Package Outline (LG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



#### Note:

1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbo		Α	A1	A2	b	D	E	E1	е	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*		0.25	0.40			<b>0</b> °	5°
	NOM	-	-	-	-	4.90	6.00	3.90	1.27 BSC -	-		0.25 BSC	-	-	
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			<b>8</b> °	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

Drawings are not to scale.

Supertex Doc. #: DSPD-8SOLGTG, Version 1041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <a href="http://www.supertex.com/packaging.html">http://www.supertex.com/packaging.html</a>.)

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<sup>\*</sup> This dimension is not specified in the JEDEC drawing.